**Lab-3: Second-order Transient Response**

In this lab we build on our analysis of the previous labs and aim to probe and analyze the response of an RLC circuit.

Objectives are:

1- Design and probe an RLC circuit in both overdamped and underdamped conditions.

2- Learn about buffers and why we need them.

**Design:**

**Step.1: Design an RLC circuit that is detectable by Arduino**

Consider the RLC circuit below. We want to observe the voltage signal on the capacitor in response to a step signal. Our objective here is to detect an under-damped response with Arduino. Remember the limitations of our scope. We cannot observe anything that happens on a time scale of less than 1ms. Ideally, I want the output to mimic Figure.1b. It should oscillate at least 3 times (Q=3), and each oscillation period must be larger than 1ms. Suppose R = 40Ω, find the appropriate bounds (lower or higher) for L and C in which the circuit is under-damped, and satisfies the criteria mentioned above (Tip: [this](https://cecas.clemson.edu/cvel/emc/calculators/RLC_Calculator/index.html) website will make your day).

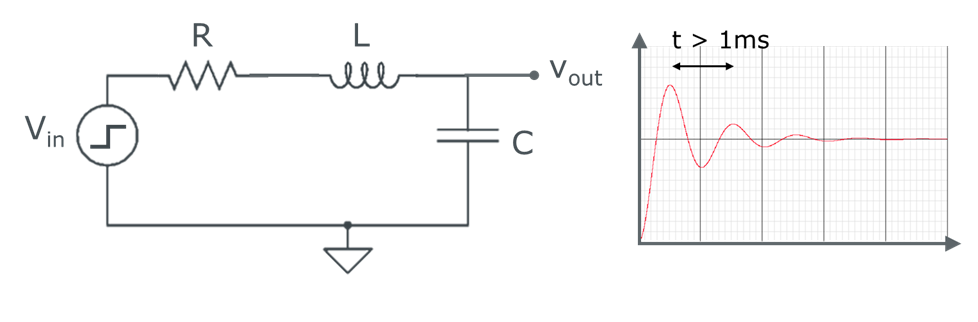


Figure.1. (a) Schematics of an RLC circuit. (b) The required output.

**Step.2: Design a voltage divider circuit (ACT-I the bad voltage divider)**

Remember the Arduino's scope limitations (I'm starting to sound like a broken record)? Our A0 pin cannot pick up any voltages beyond 5V. Since we have designed a circuit to work in underdamped condition and to hope to observe some overshoot (when signal shoots higher than 5V), we need to design a circuit that reduces the input square voltage (From 5 to 2.5). A straightforward approach can be the following circuit.

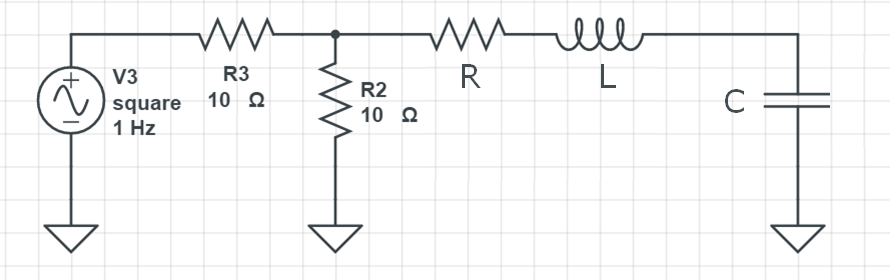




Figure.2. RLC series circuit with “bad” voltage divider.

We use a simple resistive divider to cut the signal in half. However, this is not the best design. Let's see why. Answer the following questions.

1. What are the optimal values for R2 and R3? Assume R2=R3>>R. Can this circuit still operate in underdamped condition?
2. Now assume that, R2=R3=1Ω<<R, calculate the current that will be drawn from your input signal pin (V3) when it is set at a high state (5v).
3. Check online for the absolute maximum rating for DC current through I/O pins. Do you think the previous voltage divider will be able to operate correctly?

**Step3: Design a voltage divider circuit (ACT-II the good voltage divider)**

Our main problem with the previous approach is that the RLC circuit affects the functionality of the resistor divider. These "loading effects" are a common problem in circuit design. Read the following [link](http://www.learningaboutelectronics.com/Articles/Voltage-follower#:~:text=A%20voltage%20follower%20(also%20called,any%20amplification%20to%20the%20signal.) and summarize it in one paragraph how an op-amp buffer in the following configuration will solve your design problems. Now we have our final design.



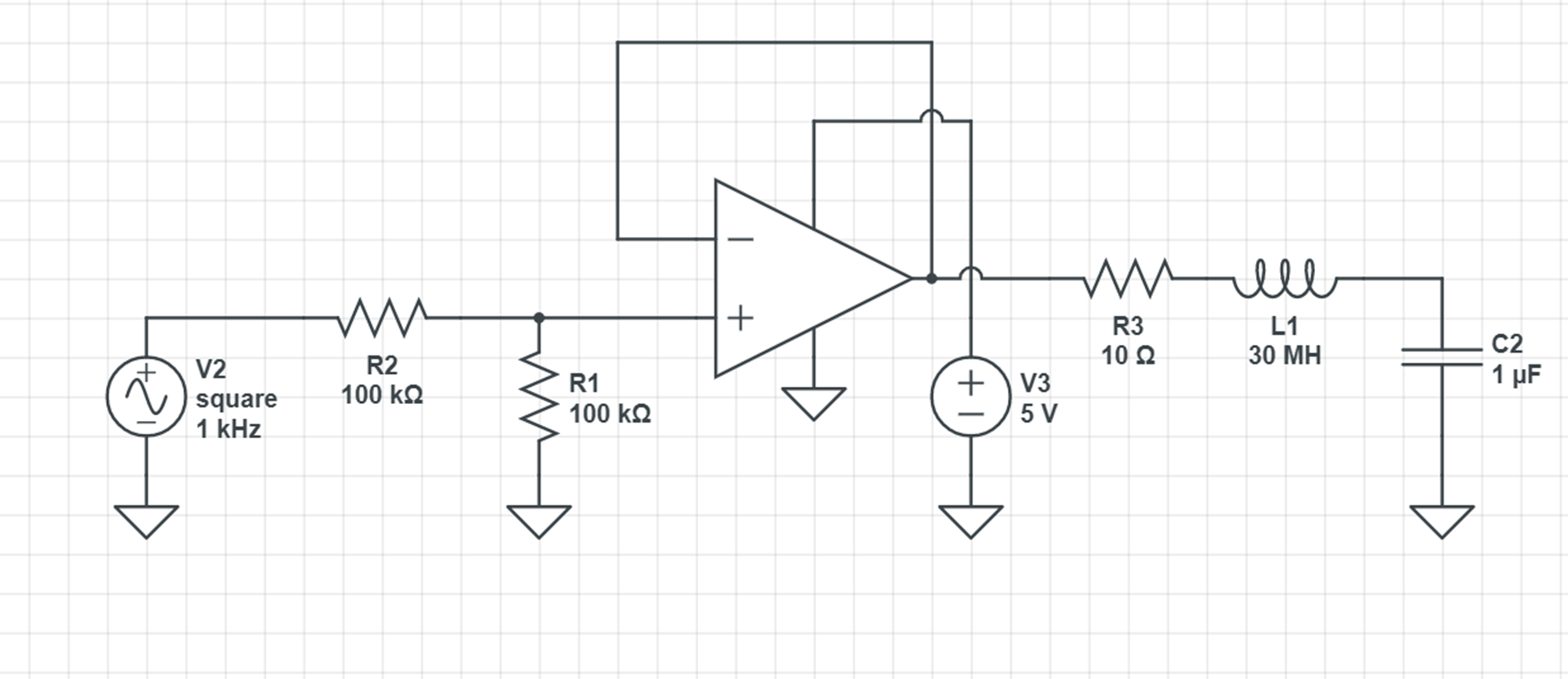


Figure.3. RLC series circuit with voltage divider followed by non-inverting op-amp buffer stage.

**Experiment:**

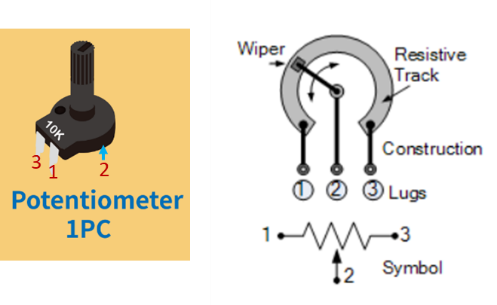
**Step.1**: Construct the RLC circuit with the non-inverting op-amp buffer configuration in Figure.3, use the following parameters (R= 10 Ω, L = 30mH, C = 3.33uF (put 3, 10uF in parallel)). Use [ALD2702](https://www.digchip.com/datasheets/download_datasheet.php?id=127990&part-number=ALD2702) CMOS op-amp chip. *(30% bonus question, you also have a TL074CN op-amp in your kit. Try this setup later with this op-amp. Why do you think the circuit is not correctly functioning using the TL074CN JFET OP-AMPs?)*. Input a 1hz square wave like the previous labs. First confirm your voltage divider functions nominally by scoping the output of the op-amp. Next, scope the voltage across the capacitor. Plot the result. Do you observe an underdamped behavior?

**Step.2:** The under-damped response oscillation period (see Figure.1, for the given parameters) of the current circuit is 1.98ms. Compared to our scope sample interval (1ms), it might be hard to observe a "text-book" under-damped oscillation. Ideally, we want the under-damped response oscillation to be larger. As we learned in the design section, this time is inversely proportional to the circuit's LC constant. Try a larger capacitor (10uF) to achieve this. Qualitatively compare the result with the result of the 3.3uF capacitor. Did the oscillation period increase as expected? Is the circuit still under-damped?

**Step.3**: Start decreasing the capacitor (Use 1uf, 680 nF and 68 nF capacitors in your kit). How does the overshoot (highest voltage reached by the under-damped signal in its first rise) changes with decreasing the capacitor? Can you find an analytical expression that describes this trend?

**Step.4:** So far, you have noticed that increasing the capacitance drives the circuit towards critically damped and over-damped conditions (decreasing the overshoot). The key to achieving an underdamped response with a long settling time (oscillation period) while maintaining a decent overshoot is to increase the inductors. However, inductors in the range of L>100mH are usually pricy (that is why we had to opt for 3x10mH inductors). Let us see why.

Let's go back to the setup of the step-1 (3.33uF capacitor). Remove the 10 Ω resistor; instead, we are going to put a potentiometer in the path (There is 10K, the potentiometer in your Arduino kits).



**[Side note 1]**: If you have not worked with one before, a potentiometer is a variable resistance. By rotating the terminal, you can change the resistance between the terminal from 0 to 10K). Note that the potentiometer has three terminals. The resistance between the front pins (leg-1 and leg-3) is always constant. The change resistance is between (leg-1 and leg-2) and (leg-2 and leg-3).

Replace the 10 Ω resistor with the potentiometer (between leg 1-2 or 2-3) in the circuit. Now start rotating the potentiometer's terminal slowly while simultaneously looking at the output of the circuit with Arduino. First, increase the potentiometer to its 10K max, which makes your system's transient response extremely over-damped. Plot the output. Now very slowly rotate the potentiometer and reduce its resistance until your circuit reaches critically damped condition. The onset in which the transient response starts to gain an overshoot is when the critically damped condition is reached. (you might need to sweep the potentiometer two-three times to find this point accurately). Plot the output in the critically damped condition. Now disconnect the circuit and calculate the resistance between the two nodes of the potentiometer. What is this resistance?

Compare this resistance with the theoretical resistance that gives you a critically damped condition. (or use this website, Find the R for which Q=0.5). After disconnecting the circuit, now measure the resistance across the three series inductors using the multi-meter.

You should notice that the inductors have ~30 Ω of resistance. Inductors' physical characteristics make it very hard to build inductors with high inductance but low internal resistance. The usual 100mH inductors typically can have about ~200 Ω of resistance. It is easy to see that even if we have used a typical larger inductor, their high internal resistance will drive the system towards an over-damped condition.

**Submission Guidelines:**

All Steps in both design and the experimental part should be addressed one by one in your report. Answer the questions that have been raised in each step. If asked to plot the scope, accompany a picture/snapshot of your scope in the response to that step. If you are making any quantitative or qualitative conclusion based on behavior of your circuit, you need to corroborate it by providing a snapshot of your scope.